Claims:

1. A network device, comprising:

   a central switch fabric subsystem including at least one local switch fabric timing subsystem;

   a distributed switch fabric subsystem coupled to the central switch fabric subsystem and including at least one local switch fabric timing subsystem; and

   a central switch fabric timing subsystem for providing a reference signal to each of the local switch fabric timing subsystems.

2. The network device of claim 1, wherein the reference signal is a segment demarcation signal.

3. The network device of claim 2, wherein the segment demarcation signal comprises a start of segment signal.

4. The network device of claim 2, wherein each local switch fabric timing subsystem generates a reference clock signal from the received reference segment demarcation signal and passes the received reference segment demarcation signal and the generated reference clock signal to switch fabric components.

5. The network device of claim 4, wherein the reference clock signal comprises a first clock period and the reference segment demarcation signal comprises a second clock period.

6. The network device of claim 5, wherein the first clock period is substantially shorter than the second clock period.

7. The network device of claim 1, wherein the central timing subsystem is located on the same printed circuit board as the central switch fabric subsystem.

8. The network device of claim 1, wherein the central timing subsystem is located on a different printed circuit board than the central switch fabric subsystem.

9. A network device, comprising:

a central switch fabric subsystem including at least one local switch fabric timing subsystem;

a distributed switch fabric subsystem coupled to the central switch fabric subsystem and including at least one local switch fabric timing subsystem;

a first central switch fabric timing subsystem providing a plurality of first timing reference signals and at least one first master control signal, wherein one of the first timing reference signals is provided to each of the local switch fabric timing subsystems;

a second central switch fabric timing subsystem providing a plurality of second timing reference signals and at least one second master control signal, wherein one of the second timing reference signals is provided to each of the local switch fabric timing subsystems;

wherein the first central switch fabric timing subsystem receives one of the second timing reference signals and the second master control signal and the second central switch fabric timing subsystem receives one of the first timing reference signals and the first master control signal; and

wherein the first central switch fabric timing subsystem synchronizes the first timing reference signals to the received second timing reference signal in accordance with the second master control signal and the second central switch fabric timing subsystem synchronizes the second timing reference signals to the received first timing reference signal in accordance with the first master control signal.

10. The network device of claim 9, wherein each of the local switch fabric timing subsystems comprise:

a phase locked loop circuit for providing a timing reference signal to local switch fabric components;

a selector circuit for receiving the first and second timing reference signals and coupled to the phase locked loop circuit; and

a control logic circuit coupled to the selector circuit for causing the selector circuit to send one of the first and second timing reference signals to the phase locked loop circuit.

11. The network device of claim 10, wherein the control logic circuit comprises a state machine.

12. The network device of claim 10, wherein each of the local switch fabric timing subsystems further comprises:

a status detector for receiving the first timing reference signal and for providing a signal to the control logic circuit indicating a status of the first timing reference signal; and

wherein, when the signal indicates that the status of the first timing reference signal is invalid, the control logic circuit causes the selector circuit to deselect the first timing reference signal.

13. The network device of claim 12, wherein when the signal indicates that the status of the first timing reference signal is invalid, the control logic circuit further causes the selector circuit to send the second timing reference signal to the phase locked loop circuit.

14. The network device of claim 12, wherein the status detector comprises an activity detector for providing an activity signal.

15. The network device of claim 12, wherein the control logic circuit causes the selector circuit to deselect the first timing reference signal without software interaction.

16. The network device of claim 9, wherein each of the local switch fabric timing subsystems further comprises:

a status detector for receiving the second timing reference signal and for providing a signal to the control logic circuit indicating a status of the second timing reference signal; and

wherein, when the signal indicates that the status of the second timing reference signal is invalid, the control logic circuit causes the selector circuit to deselect the second timing reference signal.

17. The network device of claim 16, wherein when the signal indicates that the status of the second timing reference signal is invalid, the control logic circuit further causes the selector circuit to send the first timing reference signal to the phase locked loop circuit.

18. The network device of claim 16, wherein the status detector comprises an activity detector for providing an activity signal.

19. The network device of claim 16, wherein the control logic circuit causes the selector circuit to deselect the second timing reference signal without software interaction.

20. The network device of claim 9, wherein the first and second timing reference signals comprise segment demarcation timing reference signals.

21. The network device of claim 20, wherein each local switch fabric timing subsystem generates a reference clock signal from the received reference segment demarcation signal and passes the received reference segment demarcation signal and the generated reference clock signal to switch fabric components.

22. The network device of claim 20, wherein the segment demarcation timing reference signals comprise start of segment timing reference signals.

23. A network device, comprising:

a switch fabric subsystem including at least one local switch fabric timing subsystem; and

a central switch fabric timing subsystem coupled with the local switch fabric timing subsystem for providing a reference signal to the local switch fabric timing subsystem, wherein the reference signal is a segment demarcation signal.

24. The network device of claim 23, wherein the segment demarcation signal comprises a start of segment signal.

25. The network device of claim 23, wherein the switch fabric subsystem comprises:

a central switch fabric subsystem.

26. The network device of claim 25, wherein the switch fabric subsystem further comprises:

a distributed switch fabric subsystem coupled to the central switch fabric subsystem.

27. A method of operating a network device, comprising:

providing a reference signal from a central switch fabric timing subsystem;

synchronizing a first local switch fabric timing subsystem coupled with a central switch fabric subsystem to the reference signal;

synchronizing a second local switch fabric timing subsystem coupled with a distributed switch fabric subsystem to the reference signal; and

transferring network data between the central switch fabric subsystem and the distributed switch fabric subsystem in accordance with the reference signal.

28. The method of claim 27, wherein the central switch fabric timing subsystem is a first central switch fabric timing subsystem and the reference signal is a first reference signal and further comprising:

providing a second reference signal from a second central switch fabric timing subsystem to the first and second local switch fabric timing subsystems.

29. The method of claim 28, further comprising:

detecting an error in the first reference signal;

synchronizing the first local switch fabric timing subsystem with the second reference signal;

synchronizing the second local switch fabric timing subsystem with the second reference signal; and

transferring network data between the central switch fabric subsystem and the distributed switch fabric subsystem in accordance with the second reference signal.

30. The method of claim 29, further comprising:

switching over from the first central switch fabric timing subsystem to the second central switch fabric timing subsystem.

31. The method of claim 30, wherein the central switch fabric subsystem and the first central switch fabric timing subsystem are located on the same printed circuit board and the second central switch fabric timing subsystem is located on a different printed circuit board and wherein switching over from the first central switch fabric timing subsystem to the second central switch fabric timing subsystem is transparent to the central switch fabric subsystem.

32. The method of claim 30, wherein the central switch fabric subsystem is a first central switch fabric subsystem and further comprising:

switching over from the first central switch fabric subsystem to a second central switch fabric subsystem; and

transferring network data between the second central switch fabric subsystem and the distributed switch fabric subsystem in accordance with the second reference signal.

33. The method of claim 27, wherein the distributed switch fabric subsystem is a first distributed switch fabric subsystem and further comprising:

synchronizing a third local switch fabric timing subsystem coupled with a second distributed switch fabric subsystem to the reference signal; and

transferring network data between the central switch fabric subsystem and the first and second distributed switch fabric subsystems in accordance with the reference signal.